ATTORNEY'S DOCKET NO. P94-001
PATENTS

UNITED STATES PATENT APPLICATION
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FOR

Router For Parallel Computer Including Arrangement For Redirecting Messages

Certificate of Express Mailing
Express Mail Mailing Label No. HB 158 204 475 US
Date of Deposit January 14, 1994

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By _____
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The foregoing description has been limited to a specific embodiment of this invention. It will be apparent, however, that various variations and modifications may be made to the invention, with the attainment of some or all of the advantages of the invention. It is the object of the appended claims to cover these and such other variations and modifications as come within the true spirit and scope of the invention.

What is claimed as new and desired to be secured by Letters Patent of the United States is:

Claims

1. A digital computer comprising a plurality of message generating nodes interconnected by a routing network:

A. the routing network transferring messages among said message generating elements in accordance with address information identifying a destination message generating element to receive the message;

B. each message generating node including:

i. a message data generator for generating message data items each including an address data portion comprising a destination identifier;

ii. an interface including:

a) an address translation table including a plurality of entries identifying, for at least one destination identifier, translated destination identifier;

b) a message generator for generating, in response to the receipt of a message data item from said message data generator, a message for transmission to the routing network, said message generator including an address translator for performing an address translation operation in connection with the address data and the contents of the address translation table to generate updated address data, said message generator using the updated address data in connection with generating address information for the message, the message generator coupling the message to said routing network.

2. A digital computer as defined in claim 1 in which said address translator comprises:

A. a chunk size identifier for identifying a chunk size, said chunk size identifying a number of consecutive message generating nodes;

B. a window extraction circuit for generating an address translation table entry identifier in response to said chunk size identifier and said address data and coupling address translation table entry identifier to said address translation table, the address

translation table selecting an entry in response to the received address translation table entry identifier and the original address values in said entries, said address translation table providing the translated address value from the selected entry at an output;

C. a window insertion circuit for generating said updated address value in response to said chunk size identifier, the address data and the translated address value from the output of said address translation table.

3. A digital computer as defined in claim 2 in which the address data comprises a series of address digits, said window extraction circuit generating said address translation table entry identifier as a selected series of said address digits, the window extraction circuit selecting the series of address digits in response to the chunk size identifier.

4. A digital computer as defined in claim 2 in which said address value, said updated address value and said translated address value comprise respective series of address digits, said window insertion circuit generating said updated address value by substituting the series of address digits comprising said translated address value as a selected series in the address data, the window insertion circuit selecting the digits of the address data for which it substitutes the translated address value in response to the chunk size identifier.

5. A digital computer as defined in claim 1 wherein the each message data item further includes an address mode flag having a plurality of conditions identifying the address data portion as having one of a plurality of address modes, said message generator selectively using the address data from the message data item or the updated address data from said address translator in generating a message in response to the message data item in response to the condition of the address mode flag of a message data item.

6. A digital computer as defined in claim 5 in which each message generating node is identified by a network identifier, in one address mode the address data in the address data portion of the message data item containing the network identifier of the message generating node to receive the message generated by said message generator in response thereto.

7. A digital computer as defined in claim 5 in which each message generating node is identified by a network identifier, in one address mode the address data in the address data portion of the message data item containing a relative address value identifying the difference between the network identifiers of the message generating node to receive the message and a predetermined message generating node.

8. A digital computer as defined in claim 5 in which said message generator further includes:

A. a latch;

B. an address mode flag decoder for decoding the address mode flag of a received message data item and generating an address mode signal to identify the address mode;

C. a multiplexer for selectively, in response to the address mode signal from said address mode flag decoder, coupling the address data from the message data item or the updated address data from said address translator as updated address data for storage in said latch; and

D. a control circuit for controlling storage of updated address data from said multiplexer in said latch.

9. A digital computer as defined in claim 8 wherein:

A. said address translation table provides an translated address value to said address translator in response to a translation enabling signal, and generates a translated address value valid signal when the translated address value provided to said address translator is valid; and

B. said control circuit includes:

i. an address translation table control circuit for selectively generating said translation enabling signal in response to said address mode signal;

ii. a latch control circuit for generating, in response to said address mode signal and the translated address value valid signal from said address translation table, an enabling signal for enabling said latch to store the updated address data from said multiplexer.

10. A digital computer as defined in claim 9 in which said latch has an output terminal connected to couple the contents of said latch an updated address value processing stage, said updated address value processing stage generating an advance control signal for controlling the coupling of the contents of said latch thereto, said address translation table control circuit and said latch control circuit further operating in response to said advance control signal.

11. A digital computer as defined in claim 10 in which:

A. said message generator further includes delay indication generating means for generating, in response to a delay indication enabling signal, a delay indication to said updated address value processing stage to indicate a delay in generating an updated address value; and

B. said control circuit further includes a delay indication control circuit for generating said delay indication enabling signal in response to said advance control signal, said translated address value valid signal and said address mode signal, thereby to enable said delay indication generating means to generate the delay indication enabling signal in response to a delay by said address translation table in providing a translated address value if the address mode signal identifies a selected address mode in which the updated address data is generated in response to the translated address value.

12. In a digital computer comprising a plurality of message generating nodes interconnected by a routing network, the routing network transferring messages among said message generating elements in accordance with address information identifying a destination message generating element to receive the message, a message generating node comprising:

A. a message data generator for generating message data items each including an address data portion, the address data portion of each message data item containing address data identifying one of the plurality of message generating nodes as a destination message generating node to receive a message generated in response to the message data item;

B. an interface including:

i. an address translation table including a plurality of entries each identifying an original address value and a translated address value;

ii. a message generator for generating, in response to the receipt of a message data item from said message data generator, a message for transmission to the routing network, said message generator including an address translator for performing an address translation operation in connection with the address data and the contents of the address translation table to generate updated address data, said message generator using the updated address data in connection with generating address information for the message, the message generator coupling the message to said routing network.

13. A message generating node as defined in claim 12 in which said address translator comprises:

A. a chunk size identifier for identifying a chunk size, said chunk size identifying a number of consecutive message generating nodes;

B. a window extraction circuit for generating an address translation table entry identifier in response to said chunk size identifier and said address data and coupling address translation table entry identifier to said address translation table, the address translation table selecting an entry in response to the received address translation table entry identifier and the original address values in said entries, said address translation table providing the translated address value from the selected entry at an output;

C. a window insertion circuit for generating said updated address value in response to said chunk size identifier, the address data and the translated address value from the output of said address translation table.

14. A message generating node as defined in claim 13 in which the address data comprises a series of address digits, said window extraction circuit generating said address translation table entry identifier as a selected series of said address digits, the window extraction circuit selecting the series of address digits in response to the chunk size identifier.

15. A message generating node as defined in claim 13 in which said address value, said updated address value and said translated address value comprise respective series of address digits, said window insertion circuit generating said updated address value by substituting the series of address digits comprising said translated address value as a selected series in the address data, the window insertion circuit selecting the digits of the address data for which it substitutes the translated address value in response to the chunk size identifier.

16. A message generating node as defined in claim 12 wherein the each message data item further includes an address mode flag having a plurality of conditions identifying the address data portion as having one of a plurality of address modes, said message generator selectively using the address data from the message data item or the updated address data from said address translator in generating a message in response to the message data item in response to the condition of the address mode flag of a message data item.

17. A message generating node as defined in claim 16 in which each message generating node is identified by a network identifier, in one address mode the address data in the address data portion of the message data item containing the network identifier of the message generating node to receive the message generated by said message generator in response thereto.

18. A message generating node as defined in claim 16 in which each message generating node is identified by a network identifier, in one address mode the address data in the address data portion of the message data item containing a relative address value identifying the difference between the network identifiers of the message generating node to receive the message and a predetermined message generating node.

19. A message generating node as defined in claim 16 in which said message generator further includes:

A. a latch;

B. an address mode flag decoder for decoding the address mode flag of a received message data item and generating an address mode signal to identify the address mode;

C. a multiplexer for selectively, in response to the address mode signal from said address mode flag decoder, coupling the address data from the message data item or the updated address data from said address translator as updated address data for storage in said latch; and

D. a control circuit for controlling storage of updated address data from said multiplexer in said latch.

20. A message generating node as defined in claim 19 wherein:

A. said address translation table provides an translated address value to said address translator in response to a translation enabling signal, and generates a translated address value valid signal when the translated address value provided to said address translator is valid; and

B. said control circuit includes:

i. an address translation table control circuit for selectively generating said translation enabling signal in response to said address mode signal;

ii. a latch control circuit for generating, in response to said address mode signal and the translated address value valid signal from said address translation table, an enabling signal for enabling said latch to store the updated address data from said multiplexer.

21. A message generating node as defined in claim 20 in which said latch has an output terminal connected to couple the contents of said latch an updated address value processing stage, said updated address value processing stage generating an advance control signal for controlling the coupling of the contents of said latch thereto, said address translation table control circuit and said latch control circuit further operating in response to said advance control signal.

22. A message generating node as defined in claim 21 in which:

A. said message generator further includes delay indication generating means for generating, in response to a delay indication enabling signal, a delay indication to said updated address value processing stage to indicate a delay in generating an updated address value; and

B. said control circuit further includes a delay indication control circuit for generating said delay indication enabling signal in response to said advance control signal, said translated address value valid signal and said address mode signal, thereby to enable said delay indication generating means to generate the delay indication enabling signal in response to a delay by said address translation table in providing a translated address value if the address mode signal identifies a selected address mode in which the updated address data is generated in response to the translated address value.

Abstract Of The Disclosure

A digital computer comprising a plurality of message generating nodes interconnected by a routing network. The routing network transfers messages among the message generating elements in accordance with address information identifying a destination message generating element. Each message generating node includes a message data generator and a network interface. The message data generator generates message data items each including an address data portion comprising a destination identifier. The network interface includes a message generator and an address translation table, the table including a plurality of entries identifying, for at least one destination identifier, a translated destination identifier. The message generator, in response to the receipt of a message data item from the message data generator, generates a a message for transmission to the routing network. In generating the message, the message generator performs an address translation operation in connection with the address data and the contents of the address translation table to generate updated address data which it uses data in connection with generating address information for the message.